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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,938	12/15/2005	Ryuji Komatsu	0038-0482PUS1	4081

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BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/560,938	KOMATSU, RYUJI	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/15/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

1. Claims 1-10 are is objected to because of the following informalities:

The limitation "the inner bottom face" in line 5 of claims 1 and 5 lacks antecedent basis. What is the applicant claiming with the limitation "the inner bottom face?" The office will interpret the claimed "inner bottom face" as a bottom surface of the mounting hole. Claims 2-10 depend on claim 1 and thus contain the same error.

In line 4 of claim 5, the claimed "a component mounting hole" and "a connection terminal" have antecedent basis problems. Are these the same "component mounting hole" and "connection terminal" claimed in line 4 of claim 1, or are they a second mounting hole and a second connection terminal? The limitations need to be clearly and distinctly claimed in order to overcome the antecedent basis problems. Claims 6-10 depend on claim 5 and thus contain the same error.

Furthermore, in line 5 of claim 5, the claimed "cable layer" should be amended to "cable layer or layers" to avoid an antecedent basis issue.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Hayashi et al. (US 6,809,268).

With respect to claim 1, Hayashi teaches a substrate, in fig. 4(A), for a semiconductor device on which a circuit component can be mounted, characterized in,

that a surface (4) opposite to an element mounting surface (30) is counterbored so as to form a component mounting hole (5c) where a connection terminal (38), which will be electrically connected to the circuit component (10), is exposed (38a) in an inner bottom surface (5d) of the mounting hole (as best interpreted by the office) (col. 12, lns. 44-64).

With respect to claim 2, Hayashi teaches the substrate as set forth above in claim 1, wherein the component mounting hole (5c) is located in a semiconductor element (34) mounting area (fig. 4(A)).

With respect to claim 3, Hayashi teaches the substrate as set forth above in claim 2, wherein the circuit component (10), which is electrically connected to the connection terminal (38a), is mounted in the component mounting hole (5c).

With respect to claim 4, Hayashi teaches in fig. 4(A) a semiconductor device (1b) comprising: the substrate as set forth above in claim 3; and a semiconductor element (34) being mounted on the substrate by flip-chip connection (32 and 36).

With respect to claim 5, Hayashi teaches the substrate as set forth above in claim 1, wherein the substrate is constituted by a core plate (2) and a cable layers (16, 20, 22, 24, and 28) formed on the core plate (col. 13, lns. 7-12), and

the surface of the substrate (4), which is opposite to the element mounting surface thereof (30), is counterbored so as to form a component mounting hole (5c) where a connection terminal (38), which is formed in the cable layers, is exposed (38a) in the inner bottom surface of the mounting hole (as best interpreted by the office).

With respect to claim 6, Hayashi teaches the substrate as set forth above in claim 5, wherein the component mounting hole (5c) is located in a semiconductor element (34) mounting area (fig. 4(A)).

With respect to claim 7, Hayashi teaches the substrate as set forth above in claim 6, wherein the circuit component (10), which is electrically connected (38b) to the connection terminal (38a, 38), is mounted in the component mounting hole.

With respect to claim 9, Hayashi teaches in fig. 4(A) a semiconductor device comprising: the substrate of claim 7, and a semiconductor element (34) being mounted on the substrate by flip-chip connection (32 and 36).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi ('268) as applied to claim 7 above, and further in view of Mak et al. (US 6,222,246).

With respect to claim 8, Hayashi teaches the substrate as set forth above in claim 7, including wherein a chip capacitor (10) is mounted as the circuit component.

Thus, Hayashi is shown to teach all the limitations of claim 7 with the exception of explicitly disclosing: wherein a decoupling capacitor is mounted as the circuit component.

However, Mak teaches (fig. 1) a substrate (204) wherein the circuit component is a decoupling capacitor (270) mounted in a recess formed on surface (205), opposite the element-mounting surface (232) (col. 2, lns. 55-61; col. 3, lns. 25-27).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the substrate of Hayashi to mount a decoupling capacitor within a recess formed within the backside of a chip substrate, as taught by Mak, for the disclosed intended purpose of minimizing the inductance path length and thereby reducing the inductance induced time delay, which improves the performance of integrated circuits (col. 1, lns. 10-23; col. 3, lns. 1-4).

With respect to claim 10, Hayashi and Mak teach a semiconductor device comprising: the substrate as set forth above in claim 8, and Hayashi further teaches a semiconductor element (34) being mounted on the substrate by a flip-chip connection (36 and 32).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is 571-272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AK

ANH D. MAI
PRIMARY EXAMINER